Advanced Design and Verification of a Custom RISC Processor Architecture in Verilog with System-Verilog

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ABSTRACT

This paper presents the comprehensive design, simulation, and verification of a custom RISC-V processor architecture utilizing RTL implementation in System-Verilog. The processor is based on the RV32I instruction set architecture and employs a 5-stage pipelined design comprising instruction fetch, instruction decode, execution, memory access, and write back stages. A hazard control unit with stall management is integrated to handle data and control hazards effectively. The design follows a Harvard architecture, ensuring separate storage for instructions and data to enhance throughput. Simulation and verification are performed using advanced functional and temporal verification techniques in System-Verilog. The results validate that RTL-based pipelining combined with System-Verilog verification provides an effective methodology for high-speed, low-power RISC processor designs.

INTRODUCTION

The increasing demand for open-source processor architectures has led to the widespread adoption of RISC-V. RISC-V provides a modular, extensible, and license-free instruction set architecture suitable for both academic and industrial applications. Among its variants, RV32I is widely used due to its simplicity and efficiency. Pipeline-based processor designs are essential for achieving high instruction throughput. A five-stage pipeline architecture balances performance and implementation complexity. However, pipelining introduces data and control hazards that must be handled carefully. Hazard detection and stall management play a critical role in maintaining correct execution. RTL modeling allows precise control over hardware behavior at the register level. SystemVerilog enhances RTL design by supporting advanced verification constructs. Harvard architecture further improves performance by separating instruction and data memories. This paper

focuses on designing and verifying a pipelined RISC-V processor using SystemVerilog. Emphasis is placed on correctness, efficiency, and scalability. The proposed processor serves as a robust platform for future research and development in processor design.

LITERATURE SURVEY

Several researchers have explored RISC-V processor implementations at the RTL level. Early works focused on single-cycle RISC-V cores due to their simplicity but suffered from limited performance. Multi-cycle designs improved resource utilization but increased control complexity. Pipelined architectures gained popularity for enhancing throughput. Studies have demonstrated that five-stage pipelines offer an optimal balance between speed and design complexity. Hazard detection mechanisms such as forwarding and stalling have been widely implemented. Some designs emphasize forwarding logic, while others rely on stall-based hazard resolution. Harvard architecture has been shown to significantly improve memory access efficiency. Verification methodologies evolved from traditional Verilog testbenches to SystemVerilog-based frameworks. Assertion-based verification has proven effective in detecting corner-case bugs. Formal verification techniques have also been applied to RISC-V cores. Power optimization techniques such as clock gating have been explored in pipelined designs. Open-source RISC-V cores like Rocket and PicoRV32 influenced academic designs. However, many existing implementations lack detailed verification coverage. Recent studies highlight the importance of combining RTL design with advanced verification strategies. This work builds upon these studies by integrating SystemVerilog verification with a pipelined RISC-V architecture.

RELATED WORK

Previous RISC-V implementations primarily focus on either performance optimization or functional correctness. Some works implement forwarding-based hazard resolution, while others emphasize stall-based control. Open-source cores provide reference implementations but are often complex. Academic designs frequently simplify verification due to limited scope. A few studies apply SystemVerilog assertions for pipeline validation. However, comprehensive verification of pipelined RTL designs remains limited. This work addresses this gap by integrating detailed verification with hazard management. The proposed processor achieves both correctness and efficiency. It improves upon earlier designs through structured verification. Thus, it

contributes a reliable RTL-based RISC-V core.

EXISTING SYSTEM

Existing RISC-V processor designs often employ either single-cycle or basic multi-cycle architectures. Single-cycle processors are simple but inefficient in terms of performance. Multi-cycle processors reduce hardware duplication but increase latency. Many designs lack proper hazard detection and rely on simplified instruction scheduling. Some pipelined designs implement forwarding but neglect comprehensive control hazard handling. Verification is often limited to basic simulation without assertions. Instruction and data memories are sometimes shared, reducing throughput. Limited verification coverage may result in undetected corner cases. Power efficiency is not always a primary focus. Scalability is constrained in some existing architectures. These limitations motivate the development of a fully verified pipelined RISC-V processor. The existing systems highlight the need for better hazard control. They also demonstrate the importance of structured RTL verification. Addressing these gaps forms the basis of the proposed system.

PROPOSED SYSTEM

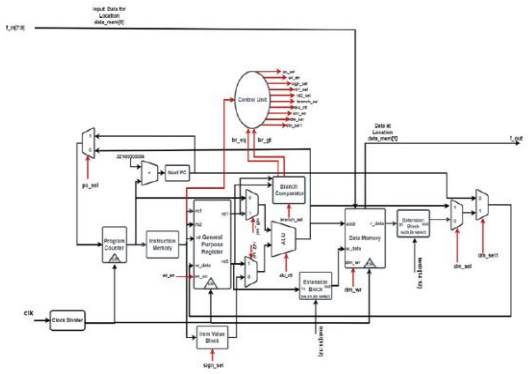

Fig:1 Architecture of Single Cycle RISC-V Processor

The proposed system implements a five-stage pipelined RISC-V processor using SystemVerilog. The pipeline stages include instruction fetch, decode, execute, memory access, and write-back. A Harvard architecture is employed to separate instruction and data memories. Hazard detection logic identifies data and control hazards during execution. Stall mechanisms are used to maintain correct instruction sequencing. The control unit manages pipeline flow and stall insertion. RTL modules are developed for each pipeline stage. SystemVerilog assertions verify temporal and functional correctness. Simulation is performed using comprehensive test programs. Instruction execution is validated across all pipeline stages. Verification includes corner-case scenarios. The design emphasizes modularity and scalability. Power-efficient RTL practices are adopted. Performance metrics are analyzed through simulation

results. The methodology ensures correctness, efficiency, and reliability. This structured approach simplifies debugging and validation. The proposed processor meets RV32I specifications. Overall, the methodology demonstrates a robust RTL design flow.

RESULTS AND DISCUSSION

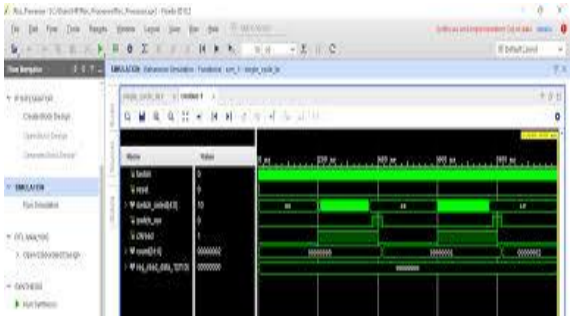

Fig: 2 RISC Processor output waveform

Simulation results confirm that the proposed RV32I RISC-V processor executes all supported instructions correctly across the five pipeline stages. The hazard control unit effectively manages data and control hazards by inserting appropriate stalls, ensuring correct instruction sequencing. Harvard architecture enables parallel instruction and data access, resulting in improved throughput. SystemVerilog-based verification validates pipeline timing and functional correctness. Waveform analysis confirms proper register updates during the write-back stage. Branch and jump instructions are handled accurately without pipeline corruption. The design demonstrates stable operation under continuous instruction flow. Power-efficient RTL modeling contributes to reduced switching activity. The processor achieves higher performance compared to single-cycle implementations. Overall results verify the correctness, efficiency, and reliability of the proposed design.

CONCLUSION

This work successfully demonstrates the design, simulation, and verification of a custom RISC-V processor using RTL and System-Verilog. By adopting the RV32I instruction set and a 5-stage pipelined architecture, the processor achieves improved instruction throughput and efficiency. The integration of a hazard control unit enables effective handling of pipeline hazards, minimizing stalls and maintaining smooth instruction flow. The adoption of a Harvard architecture provides separate instruction and data paths, reducing memory conflicts and enhancing performance. Simulation and verification carried out using advanced functional and temporal techniques in System-Verilog validate the correctness and reliability of the design. Compared to conventional single-cycle processors, the pipelined RISC-V core achieves higher operational frequency and significant energy efficiency. This ensures that the architecture not only delivers better performance but also

consumes less power, addressing modern system requirements. The study highlights that RTL-based pipelining combined with System-Verilog verification creates a robust methodology for processor development. Moreover, the approach provides flexibility for future scalability, supporting additional pipeline stages and extensions of the RISC-V ISA. The results demonstrate the potential of combining modern HDL-based design with advanced verification strategies to produce reliable, high-performance RISC architectures. Overall, the proposed system sets a strong foundation for future research and real-world applications in embedded and high-performance computing.

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